REMARKS

The Examiner's Advisory Action mailed on September 23, 2004, has been received and its contents carefully considered.

Claims 1-20 are currently pending in this application. Claims 1, 6 and 14 are independent claims, and are each amended herein.

The Applicant wishes to acknowledge with appreciation the Examiner's indication in the present Action that claims 2-5 and 10 would be allowable if rewritten in independent form to include all the limitations of their respective base claims and any intervening claims.

In the Action, claims 1, 6, 9, 11, 12-14 and 17-20 are rejected under 35 USC §103(a) as being obvious over Minami (U.S. Patent No. 5,402,446) in view of Kim (U.S. Patent No. 5,854,876). Claims 7, 8, 15 and 16 are rejected under 35 USC §103(a) as being obvious over Minami in view of Kim, and further in view of Suzuki et al. (U.S. Patent No. 6,522,665). Independent claims 1, 6 and 14 are amended herein to more clearly distinguish over the applied references.

The present invention is directed to a receiving circuit for storing and outputting a pseudo random pattern included in demodulated digital data (see, for example, specification at page 15, line 25 through page 16, line 10). A bit error rate characteristic is measured by counting the received pseudo random pattern (see, for example, specification at page 3, lines 8-22). In order to output the pseudo random pattern, the receiving circuit has a detector to detect a synchronization pattern from the demodulated data. The present invention is capable of outputting the pseudo random pattern even for data bursts in which the synchronization pattern is not detected (see, for example, specification at page 15, lines 20-25). Independent claims 1, 6 and 14 are amended herein to clarify the above-discussed features of the invention.

In the Action, the Examiner points to the combination of Minami and Kim as disclosing the features recited in the independent claims. With regard to claim 1, for example, the Examiner asserts that Minami discloses, among other things, "a pulse generator capable of receiving the instruction signal (Minami fig. 1: 18 receives output of 16) and outputting a pulse signal each time a predetermined time elapses since the

reception of the instruction signal …; a control circuit which outputs control signals corresponding to at least either one of the instruction signal and the pulse signal (Minami fig. 1: output of 22 is based on 18); and a clock generator (Minami fig. 1: 20) which generates a clock signal (Minami fig. 1: output of 20) for storing an outputting desired data included in the demodulated data (Minami fig. 1: multiple elements in fig. 1 store and output as claimed such as sample and hold circuit 52) in response to the control signal (Minami fig. 1: the outputs of elements in fig. 1 are in response to the control signal output from 22)."

The Applicant disagrees with the Examiner's characterization of the teachings of Minami. For example, the Examiner asserts that the intermittent driving circuit 18 of the Minami invention corresponds to the pulse generator recited in claim 1. However, the function of the intermittent driving circuit 18 is to produce a VCO on/off signal and a PLL on/off signal for the PLL local oscillator 10 of Minami Fig. 1, both signals indicating ON at a leading time earlier than a data taking-in time for a desired time slot, thus allowing for a margin for phase lock pull-in time in the PLL local oscillator 10 (column 6, lines 57-63). Thus, the intermittent driving circuit 18 in Minami does not produce a pulse signal that has anything to do with controlling the storing and outputting of the demodulated data, as in the present invention. Moreover, the output signals of the intermittent driving circuit 18 do not occur at a predetermined time after the reception of the instruction signal, as claim 1 would require, but rather at different times depending on the presence or absence of a control signal FL, which indicates whether the voltage controlled oscillator 20 in the PLL local oscillator 10 has a small frequency error in its free running state (column 7, lines 1-16).

The Examiner also incorrectly associates the PLL circuit 22 with the control circuit recited in claim 1. The first difference between the two is that PLL circuit 22 is disclosed as only having one signal input to it, the PLL on/off signal (Minami Fig. 1), while the claimed control circuit receives both the instruction signal from the detector and the pulse signal from the pulse generator, and performs a logical OR function, i.e., "outputs control signals corresponding to at least either one of the instruction signal and the pulse signal." Secondly, Minami lacks any suggestion that the PLL circuit 22 "outputs control signals" in response to which a clock generator "generates a clock signal for storing and outputting a

pseudo random pattern included in the demodulated data," as claim 1 would require. Rather, the PLL circuit 22 is disclosed as connected to the voltage controlled oscillator 20 so as to produce a phase difference signal in response to the voltage controlled oscillator signal and a reference oscillator signal (column 3, lines 12-16, and Fig. 2).

Further, the Examiner asserts that VCO 20 in Minami corresponds to the clock generator recited in claim 1, which generates a clock signal for storing and outputting desired data included in the demodulated data, and asserts that Minami includes multiple elements for storing and outputting as claimed, such as sample and hold circuit 52.

This aspect of the Examiner's analysis is problematic in at least two respects. First, the function of VCO 20 is to generate a first local oscillator signal for the dual conversion receiver described in Minami. There is no suggestion, contrary to the Examiner's position, that the output of VCO 20 is a clock signal that used in any way in storing and outputting any of the demodulated data. The output of the VCO is connected to the first mixer 32, and not to any of alleged storage elements in the Minami receiver. Second, contrary to the Examiner's assertions, Minami fails entirely to disclose any elements for storing and outputting any portion of the demodulated data, which appears in Minami at the output of decision circuit 48 (column 4, lines 35-37). The function of the sample and hold circuit 52, to which the Examiner refers, is to sample and hold an integrated signal at the output of integration circuit 50, which represents the DC value of the demodulated signal, and is indicative of the deviation from a phase lock in the phase locked loop (column 4, lines 39-62). Clearly, there is no demodulated data at the output of the sample and hold circuit 52.

In the Action, the Examiner acknowledges that Minami fails to teach a detector which detects a synchronizing pattern included in the demodulated data and outputs an instruction signal for providing instructions for a result of the detection, as the claims recite. The Examiner points to Kim as teaching this feature (Fig. 1: 16 and column 5, lines 12-18), and argues that it would have been obvious to one skilled in the art at the time of the invention to modify the Minami synch circuitry with the teachings of the Kim synch system.

Without addressing the merits of the Examiner's arguments regarding Kim, it is respectfully submitted that Kim fails to address any of the other deficiencies noted above in

the base reference, Minami, so that the teachings of Kim and Minami, even if combined as suggested by the Examiner, would not produce the claimed invention.

In the Action, independent claims 6 and 14 are rejected for very much the same reasons as claim 1. Accordingly, it should be clear without further elaboration that claims 6 and 14 also distinguish over the applied art references. The Applicant also believes that the independent claims are further distinguished by addition of the express limitation regarding "storing and outputting a pseudo random pattern included in the demodulated data," a feature that does not appear to be taught by any of the applied references.

In summary, it is respectfully submitted that independent claims 1, 6 and 14 as now amended, as well as dependent claims 7-9, 11-13 and 15-20, patentably distinguish over the applied art references, whether considered individually or in combination. Allowance of the application with claims 1-20, and passing of this case to issue are earnestly solicited.

Should the Examiner believe that an interview would be helpful in resolving any open issues regarding this application, the Examiner is respectfully invited to call the undersigned attorney to schedule such an interview.

Respectfully submitted,

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